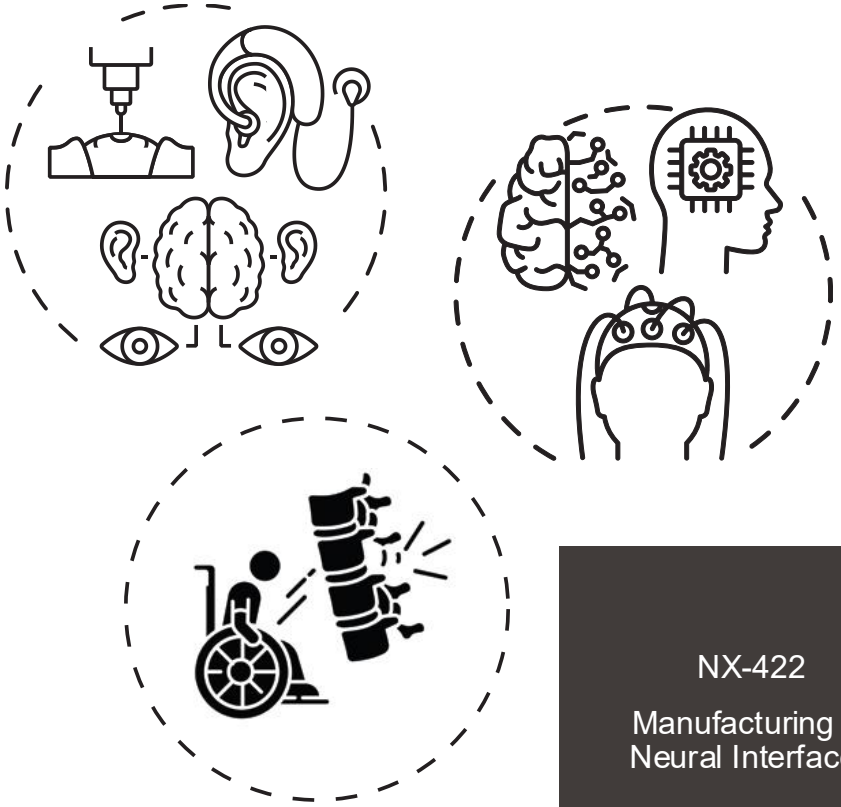


Neural Interfaces

NX-422

Manufacturing of Neural Interfaces

Giuseppe Schiavone

Neuro-X Institute

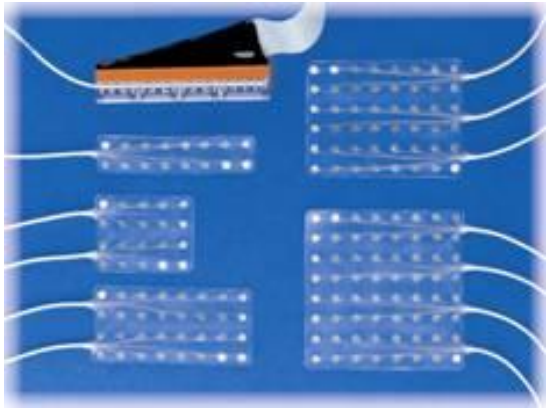
Neural interfaces manufacturing

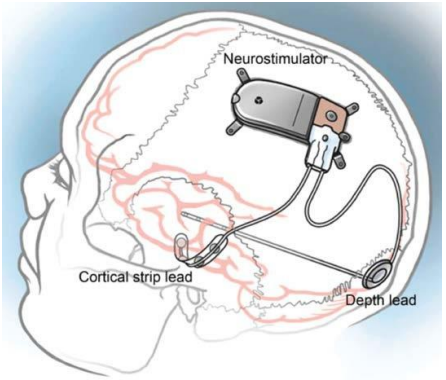
- Overview
- Silicon-based neurotechnology
- Flexible implantable neurotechnologies

Invasive BCI / in the clinic

ECoG grids

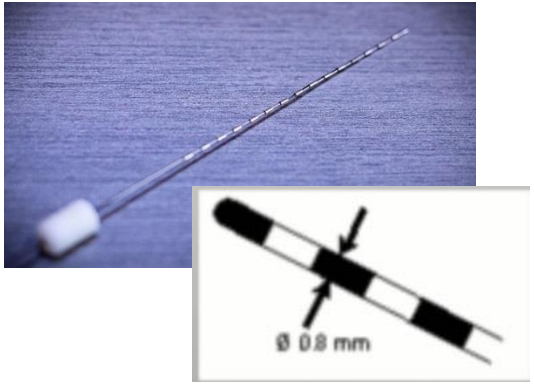
Adtech





NeuroPace, USA

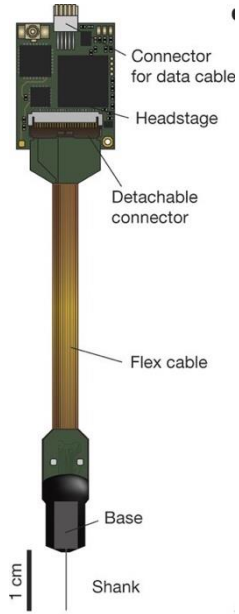
sEEG



Clinatec ECoG, CEA, France

Invasive BCI / short-mid- term use in the clinic

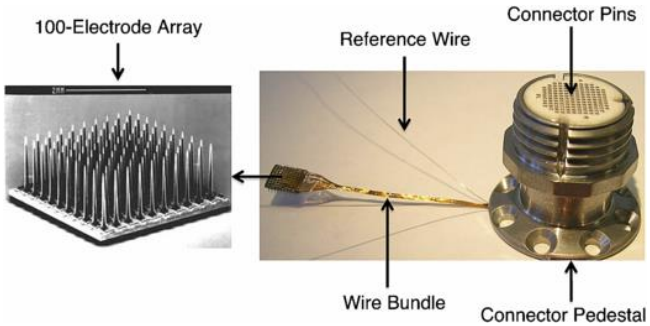
Neuropixel – IMEC Janelia



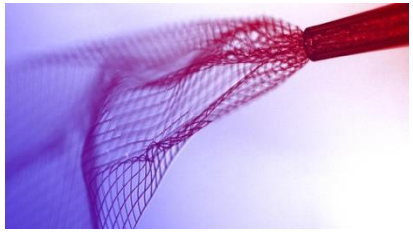
Synchron – stentrode

Utah array
BrainGate

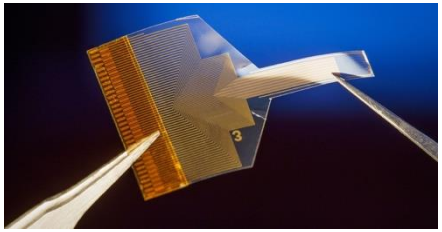
Blackrock Neurotech



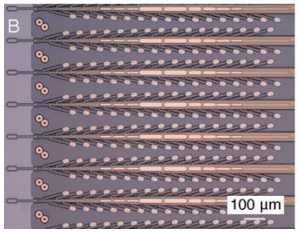
Miniaturised BCI

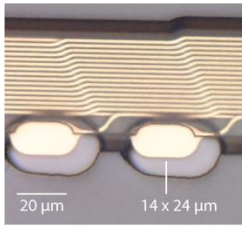


Nanomesh
Jia Liu - Harvard



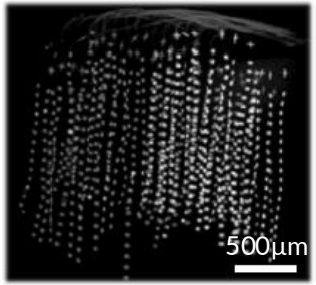
transparent ECoG
D Kuzum- UCSD





Neuralink

soft ECoG
SP Lacour – EPFL / Neurosoft Bioelectronics

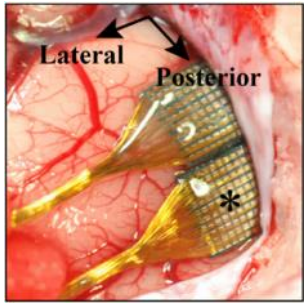


NET 1’024 électrodes
L. Luan, Rice Univ.

graphene electrodes
InBrain - Spain

All about connectors

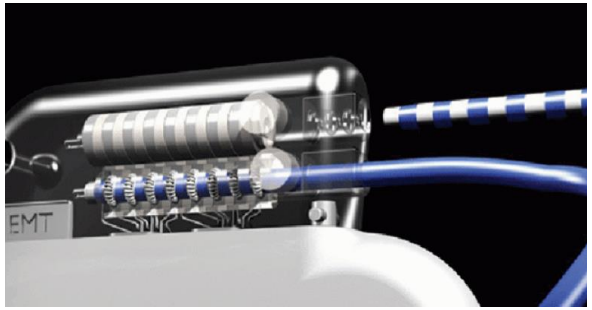
BrainGate



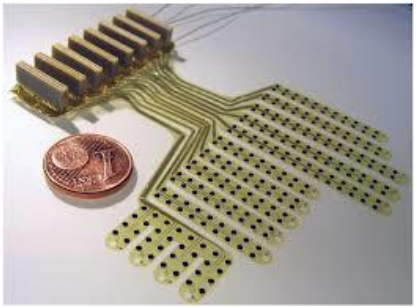
JNE | 2012 | 9(6)

Transcutaneous interface
Wire bonding

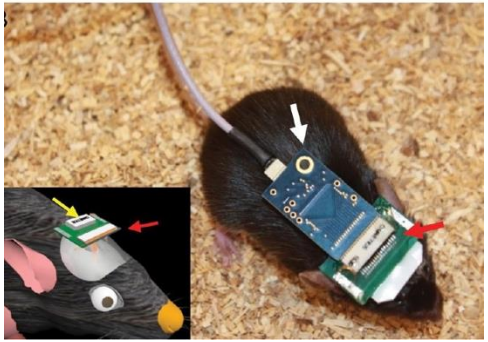
Utah implant system



Bal seal Engineering Inc.

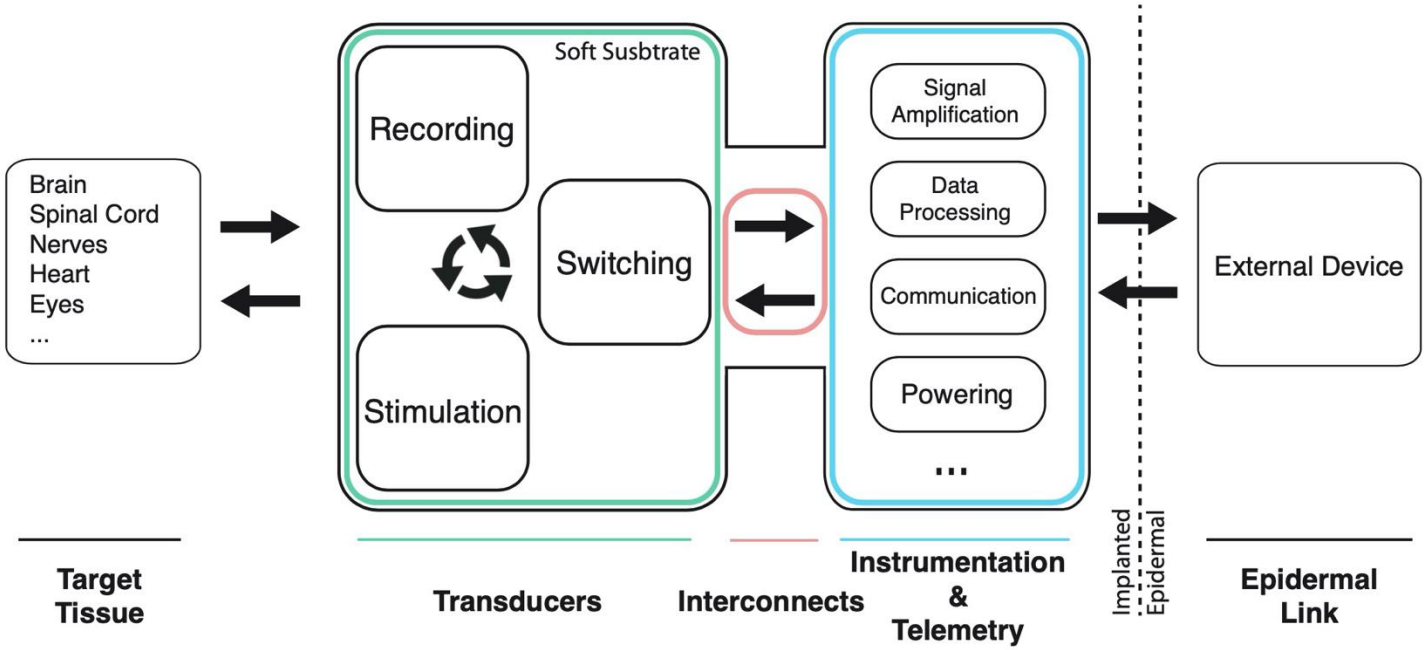


Flexible ECoGs
T. Stieglitz's lab



Nanomesh connector
C. Lieber

Architecture of an implantable bioelectronic system



Fallegger et al. 2019

Example

Neural interfaces

Interconnections

Implanted electronics

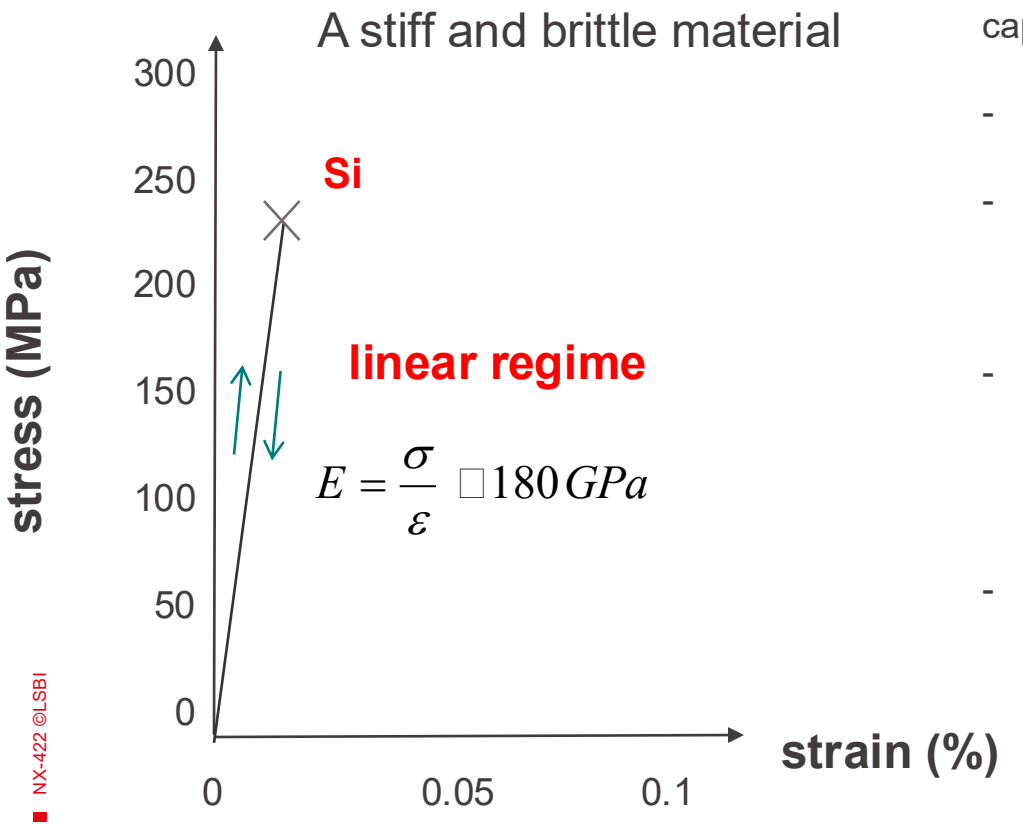
Hermetic packaging

CorTec GmbH

Neural interfaces manufacturing

- Overview
- **Silicon-based neurotechnology**
- Flexible implantable neurotechnologies

Silicon

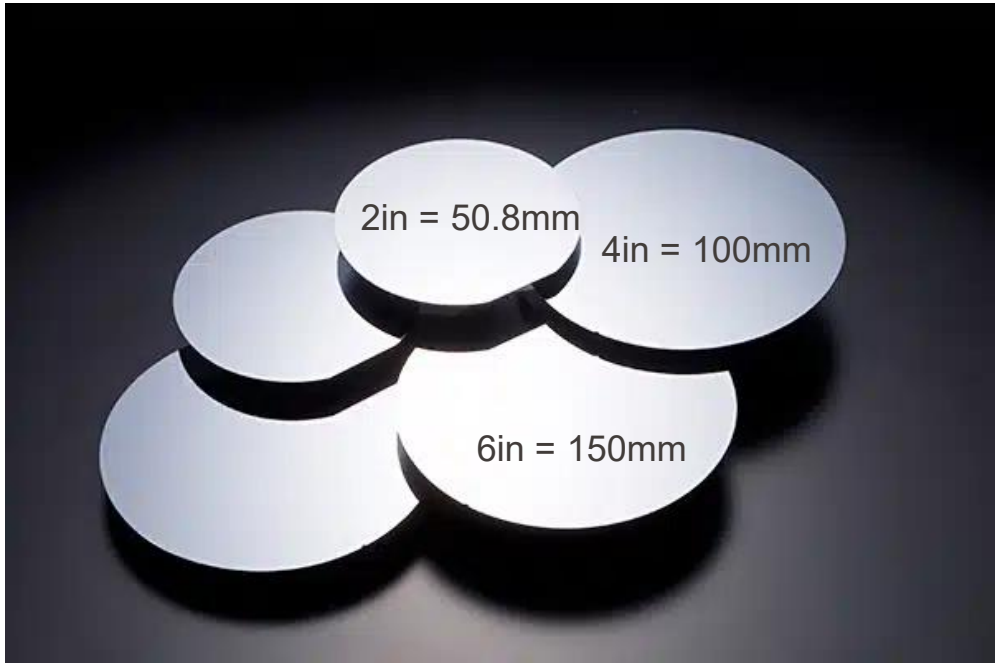


"Inherited" from μelectronics because of the CMOS capabilities (doping)

- Excellent control over the mechanical properties.
- **Thermal stability:** High melting point and good thermal conductivity make it robust through high-temperature steps (oxidation, diffusion, anneals).
- **Surface chemistry control:** Surfaces can be precisely cleaned, passivated, and functionalized; $Si/SiO_2/Si_3N_4$ stacks are well understood for adhesion and protection.
- **Scale & cost:** Abundant material, mature equipment and supply-chain. Decades of CMOS know-how transfer directly to MEMS.

Silicon wafers

- diameter: 2in – 18in
- *12in: modern semicond. fab.*
- thickness: 275 - 1’000 µm
- flatness
- orientation flat and notch
- *(100) or (111) orientation*
  (anisotropicity in some properties)



Microfabrication in a Cleanroom a highly controlled environment

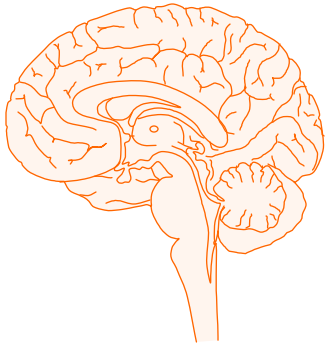
- **Classification ISO**
  - ISO class 1: 10 particles per m^3 (particles > 0.1µm)
  - ISO class 5: 100'000 particles per m^3 (particles > 0.1µm)
- **Air filtration**
- **Temperature and humidity control**
- **Surface cleanliness**

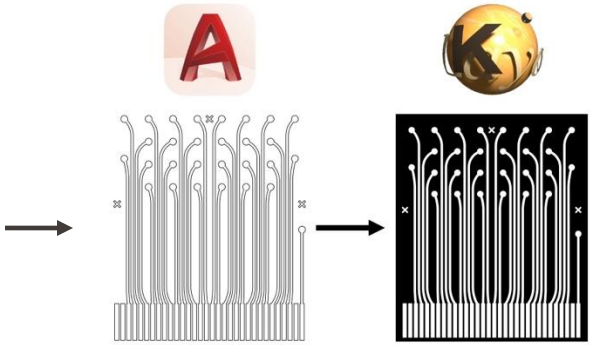
Class	≥0.1 µm	FED STD 209E equivalent
ISO 1	10[b]	
ISO 2	100	
ISO 3	1,000	Class 1
ISO 4	10,000	Class 10
ISO 5	100,000	Class 100
ISO 6	1,000,000	Class 1,000
ISO 7	[c]	Class 10,000
ISO 8	[c]	Class 100,000
ISO 9	[c]	Room air

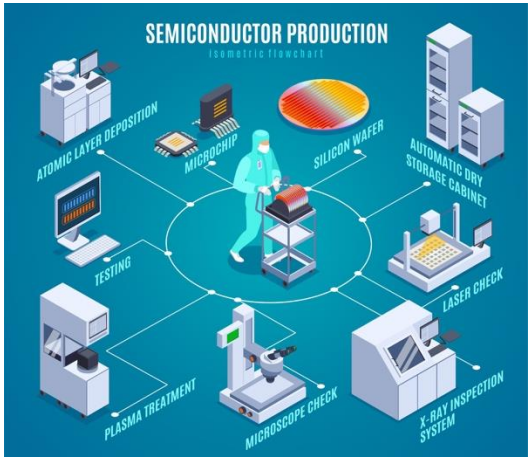
https://en.wikipedia.org/wiki/Cleanroom#ISO_14644-1_and_ISO_14698

Microfabrication in a Cleanroom a highly controlled environment

microfabrication







1. Imaging

2. Design

3. Manufacturing

Layer-by-layer fabrication – subtractive

- **Build 3D by stacking 2D.** Start with flat wafer, then add a thin film, pattern it, etch it, and repeat. Layer-by-layer steps turn flat patterns into 3D devices.
- **Add material.** Grow/deposit films (metals, SiO_2, Si_3N_4), via thermal oxidation, CVD, PVD, ALD.
- **Pattern with lithography.** Spin photoresist, align to marks, expose (UV), develop → a temporary mask defining where the **underlying** layer stays or goes.
- **Transfer the pattern.** Remove material with etching (dry RIE for vertical sidewalls; wet for isotropic). For lift-off for metals, special litho before deposition.
- **Clean, inspect, control.** Strip resist, clean residues, and use metrology (ellipsometry, SEM, etc.) to ensure each layer is in spec.

Layer-by-layer fabrication – additive

- **Build 3D by stacking 2D.** Start with flat wafer, then selectively add thin (thick?) films where needed through a patterned mask.
- **Pattern mask with lithography.** Spin photoresist, align to marks, expose (UV), develop → a temporary mask that defines where the **next** layer goes.
- **Add material.** Grow/deposit films through the mask, via electrodeposition, printing, etc.
- **Clean, inspect, control.** Strip resist, clean residues, and use metrology (ellipsometry, SEM, etc.) to ensure each layer is in spec.

Materials

- **thin-films**
  - metals
  - insulators
- deposition
  - evaporation
  - sputtering
  - ALD
  - CDV…
- etching

sputterer

evaporator

Materials

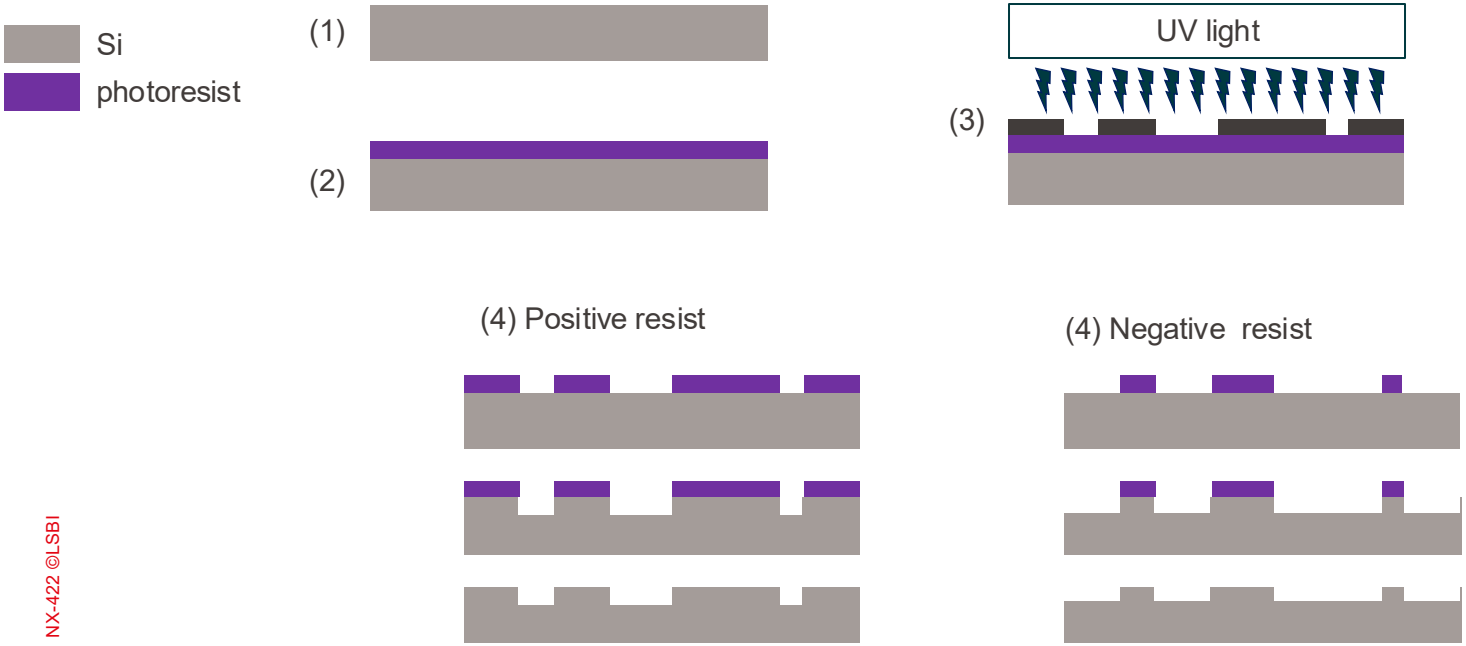
- **photoresists**
  - positive
  - negative

- parameters
  - Thickness range: 0.5 - 2 µm (thin)
  - Thickness range: 2 - 100 µm (thick)
  - spin-coating speed
  - Sensitivity (dose needed) vs resolution (smallest feature)
  - Contrast (sharpness of transition btw soluble/insoluble)
  - DUV to UV sensitive
  - E-beam and X-ray
  - Etch resistance
  - Adhesion
  - ...

coater - developer

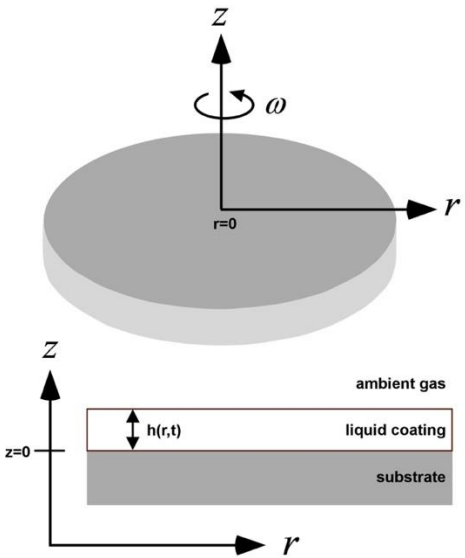
Photolithography

- Transfer of a geometric pattern through a photomask into a photosensitive polymer

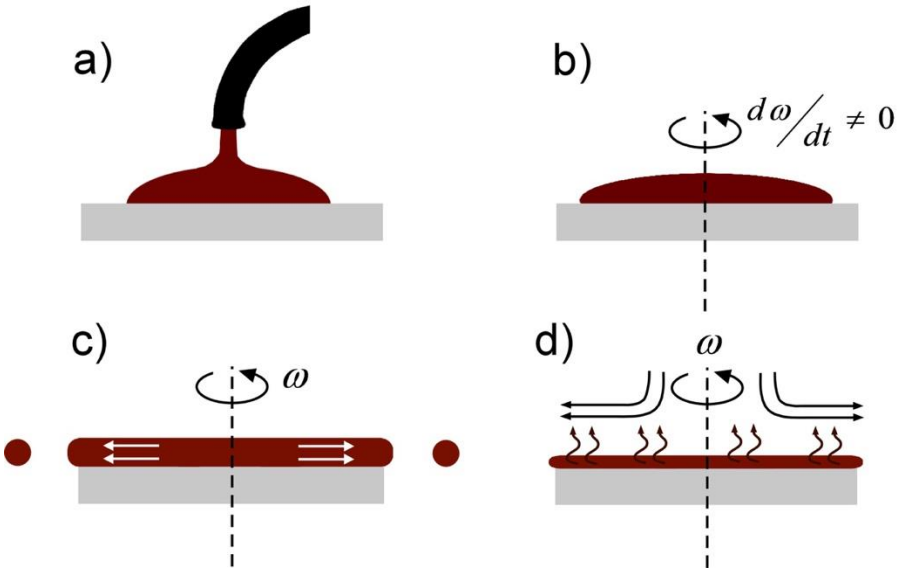


Spin-coating

Viscous fluid on a rotating disk



Dispense / Accelerate / Flow / Evaporate

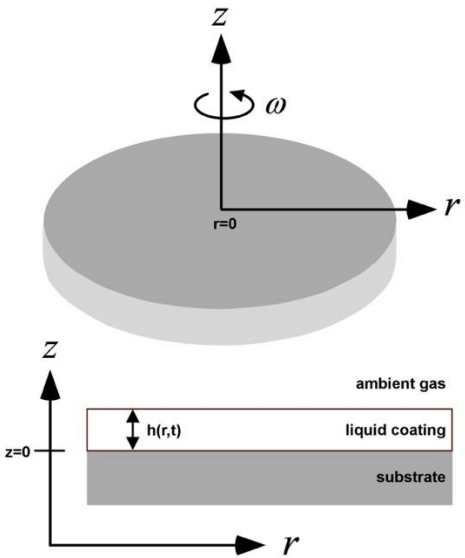


https://www.youtube.com/watch?v=uv1A7qAqgRk

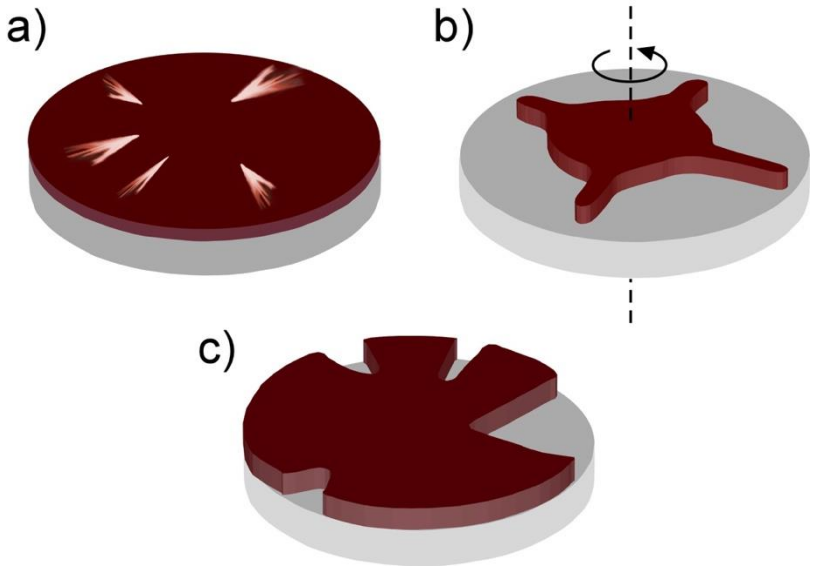
Adapted from S.L. Hellstrom, Stanford University

Spin-coating

Viscous fluid on a rotating disk



Deviation from ideal spin
Streaks / Non uniformity / uncoated areas



Goal: uniform thickness controlled by spin speed only (not time, volume, …)

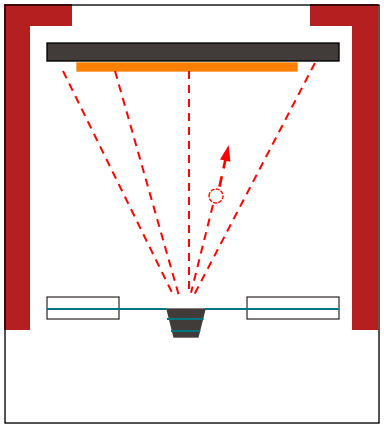
Adapted from S.L. Hellstrom, Stanford University

Metallization

Process parameters:

- Pressure
- Temperature
- Deposition rate

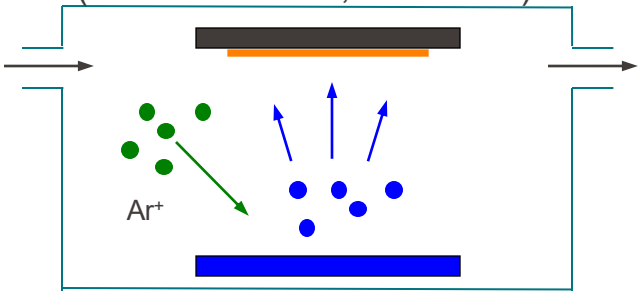
Evaporation



www.lesker.com

Sputtering

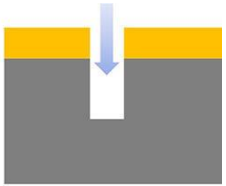
Also used for a wide range of inorganic materials (semiconductors, dielectrics)



Etching

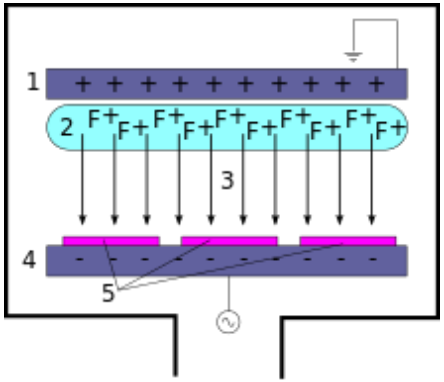
- Wet etching
  - Selective, isotropic
  - e.g. KOH for Si

Isotropic Etching

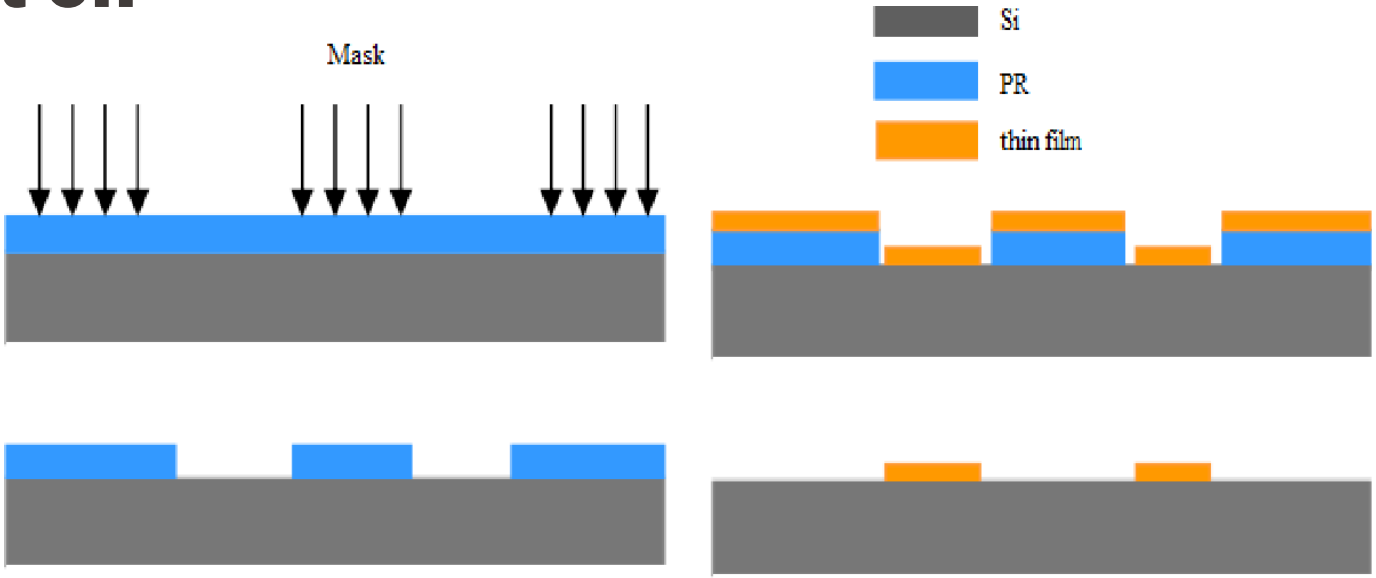


Anisotropic Etching

- Dry etching
  - usually selective, anisotropic
  - e.g. reactive ion etching (RIE) (chemical + physical)
    - low-pressure plasma to remove material directionally
  - (also vapour etch, no plasma)
    → see MEMS surface micromachining…



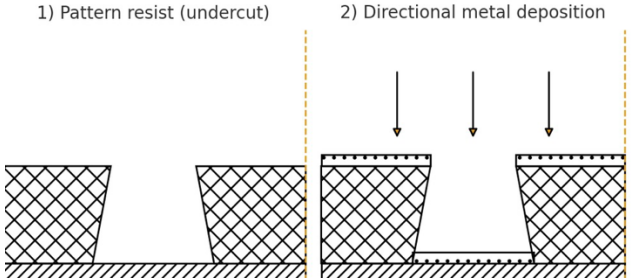
Lift-Off



DOI:10.51847/7tmarkoorg

Figure 1. Lift-off process

→ Avoids etching step
→ Requires careful photoresist profiling and ~directional (non-conformal) thin-film deposition



Some Typical processes

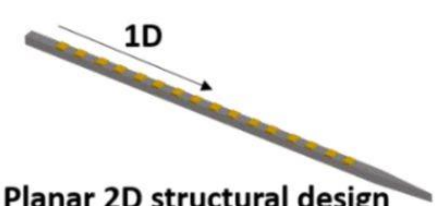
Material	Thin-film deposition	Patterning (typical)	Notes
Silicon (Si)	• **Epitaxial CVD** (SiH_4/SiH_2Cl_2 + H_2) • **LPCVD polysilicon** • **PECVD a-Si** • **Sputter/evap** (amorphous)	• **Dry:** RIE/ICP (SF_6, HBr/Cl_2), **DRIE (Bosch)** for deep high-AR • **Wet: KOH/TMAH** (anisotropic), **EDP** (legacy), **HNA** (HF–HNO_3–CH_3COOH, isotropic)	Orientation matters for wet etch (e.g., {111} slow). Use hard masks for deep Si etches.
Silicon dioxide (SiO_2)	• **Thermal oxidation** (dry/wet) • **LPCVD/PECVD/HDPCVD** • **ALD SiO_2** • **Sputter/evap**	• **Dry:** Fluorocarbon RIE (CF_4/CHF_3/C_4F_8 + O_2) • **Wet: HF**, **BOE (HF/NH_4F)**	Photoresist masks OK for short etches; for long/harsh etches use Si_3N_4 or metals as hard masks.
Gold (Au)	• **Evaporation (e-beam/thermal)** • **Sputtering** • **Electroplating** (needs seed) • **Electroless Au** (select chemistries) • (ALD exists but specialized)	• **Patterning: Lift-off (preferred)** • **Wet etch: KI/I_2** or **aqua regia** • **Dry/physical: Ion beam etch (IBE/milling)**; Cl_2/Ar RIE possible but tricky	Use **Cr or Ti adhesion** underlayers; wet etches attack Cr/Ti differently—plan the stack/removal order.
Platinum (Pt)	• **Sputtering** • **E-beam evaporation** • **ALD Pt** (e.g., $MeCpPtMe_3$ + O_2) • **Electroplating** (special baths)	• **Patterning: Lift-off** (common) • **Physical: Ion beam etch/milling** • **Dry:** Cl_2/Ar or halogen-based RIE (slow, process-sensitive) • **Wet: Hot aqua regia/oxidizing halide** mixes (slow)	Pt is hard to etch chemically; expect slower rates and more redeposition—plan for IBE or lift-off.

The process flow
a detailed sequence of steps and techniques

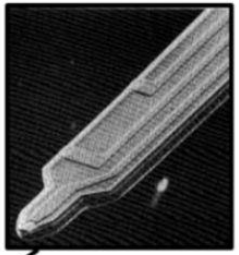
→ a roadmap outlining how various fabrication processing are combined to create the desired features on a silicon wafer

- **Recipe:** To define the roadmap.
- **Repeatability**: To ensure that devices are fabricated consistently with high yield.
- **Optimization**: To minimize defects and improve performance.
- **Documentation**: Provides a clear record of every step and parameter, essential for troubleshooting and improving processes.

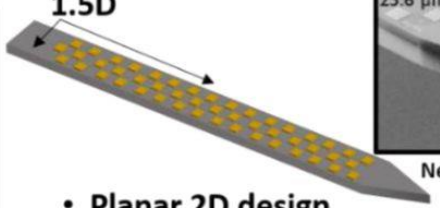
Silicon-based electrodes

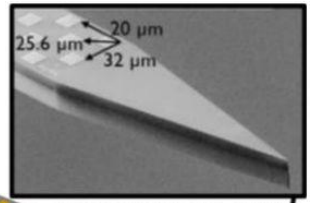


- Planar 2D structural design
- 1D sites spatial coverage
- Example: Michigan Probe



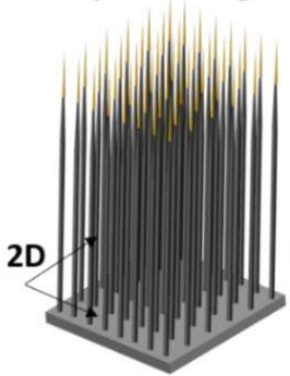
Michigan Probe, 1985

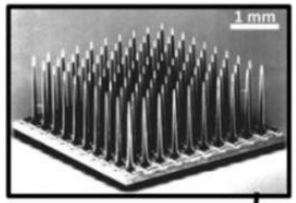




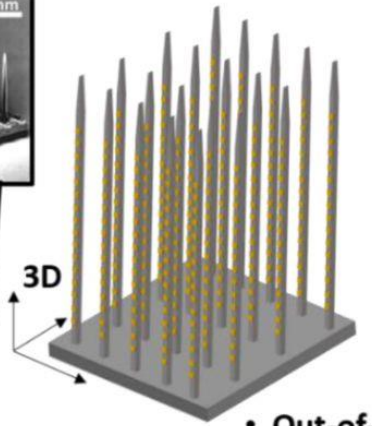
Neuropixel Probe, 2017

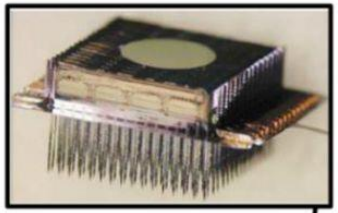
- Planar 2D design
- 1.5D sites spatial coverage
- Example: Neuropixel (IMEC Probe)





Utah Electrode Array, 1991





Michigan 3D Array, 1991

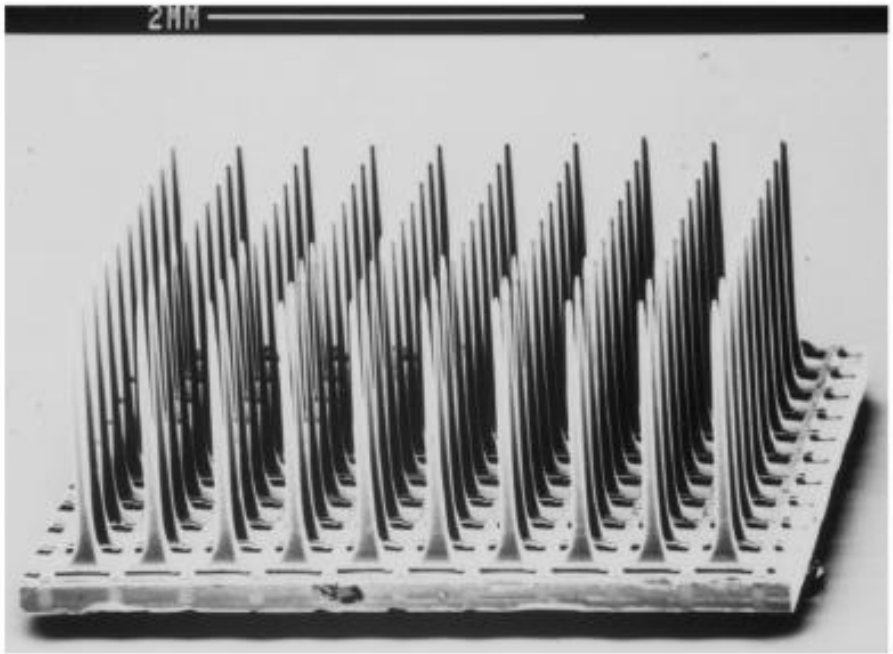
- Out-of-Plane 3D structural design
- 2D sites spatial coverage
- Example: Utah Electrode Array

- Out-of-Plane 3D structural design
- 3D sites spatial coverage
- Example: Michigan 3D Array

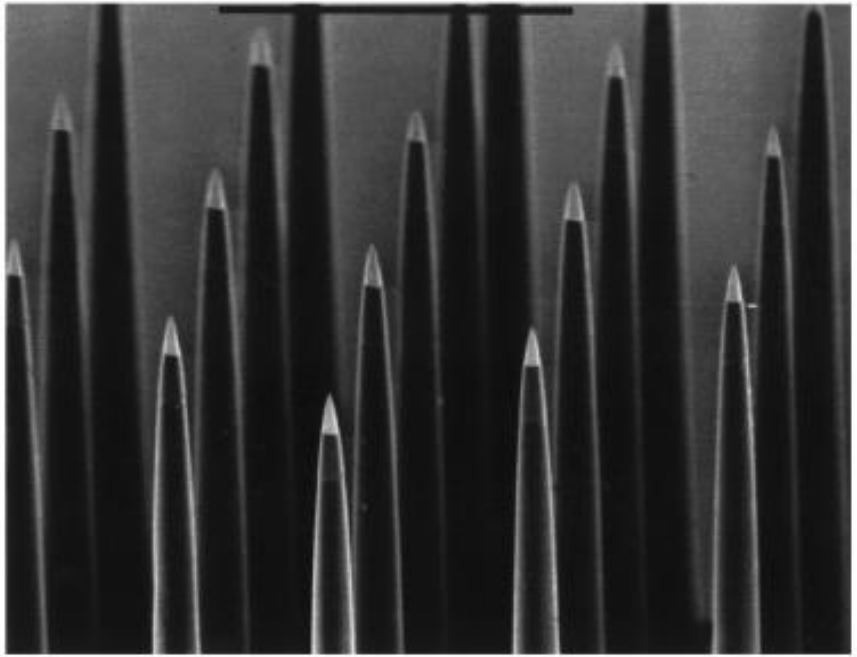
https://doi.org/10.1101/2021.01.24.427975

The Utah array

Biomed Microdevices (2010) 12:797–807

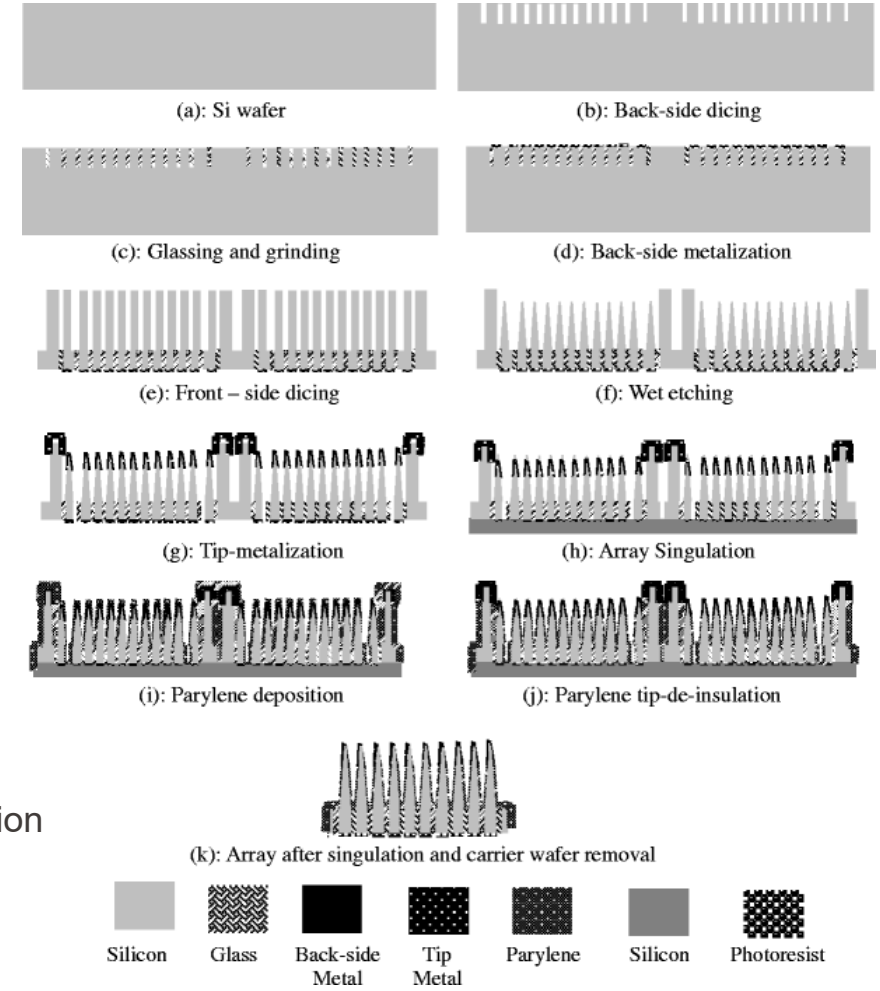


(a)



(b)

The Utah array



a. Backside dicing
→ 10x10 0.5mm deep matrix

b. **Glassing**

c. **Grinding**

d. **Back-side metallization**
→ Pt/TiW/Pt sputtering

e. **Front-side dicing**
→ 1.5mm deep columns

f. **Wet etching**
→ HF:HNO_3 (1:19 ratio)

g. **Tip metallization**
→ sputtered Ti/Ir then electrochem. activation

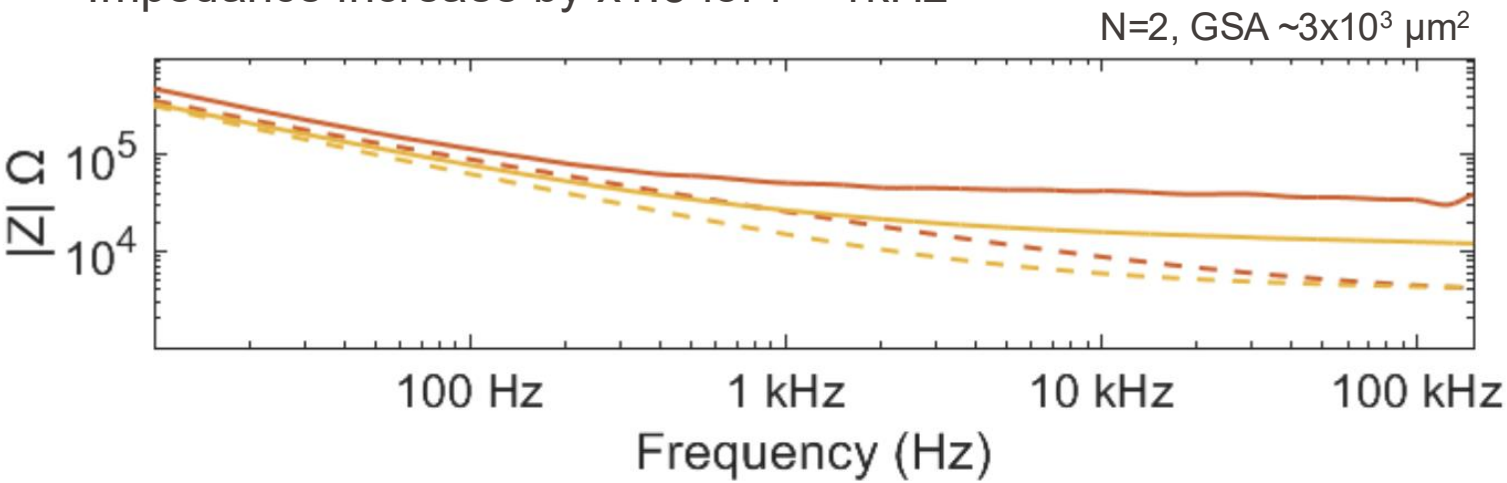
i. **Parylene deposition**
→ LPCVD, 3µm thick

j. **De-insulation**
→ oxygen plasma etching, 30-350µm length

Biomed Microdevices (2010) 12:797–807

Measured impedance spectra

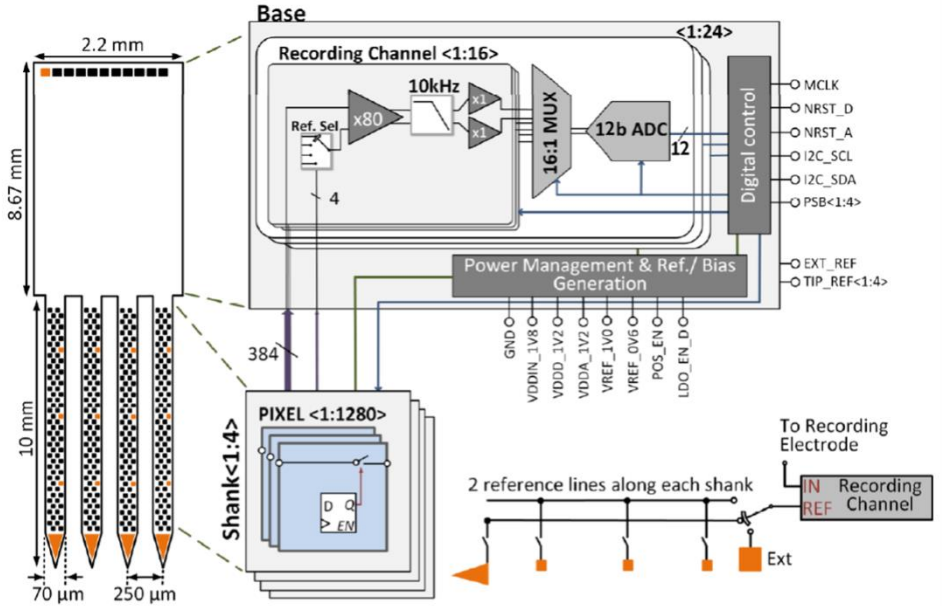
- In vitro electrodes (dashed)
- In vivo electrodes (plain)
- Impedance increase by x1.5 for f > 1kHz



10.1109/JERM.2018.2862417

Active silicon probes
Neuropixel

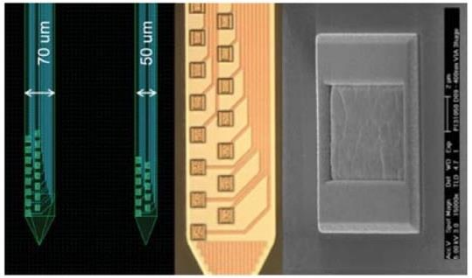
user-programmable switches that allow the recording channels to address 384 of the **960 total sites** simultaneously
130nm CMOS technology

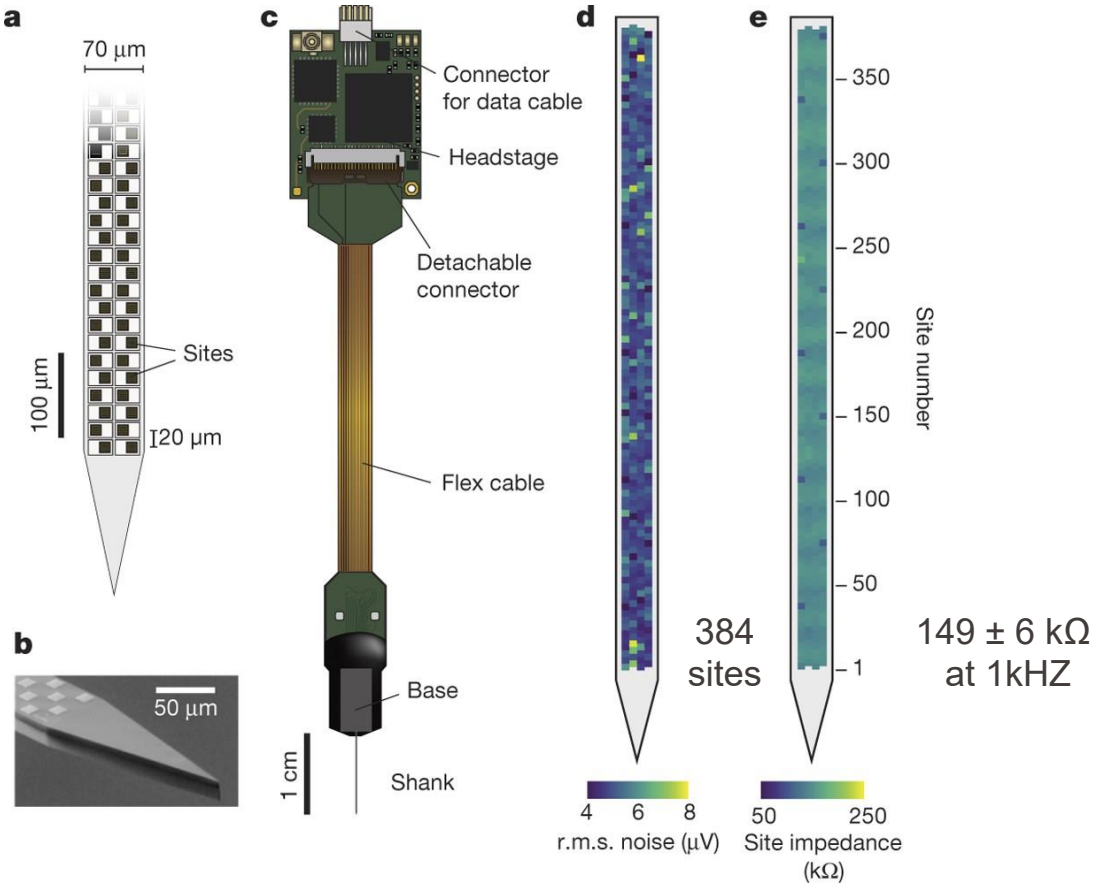


IMEC

Active silicon probes
Neuropixel

TiN coating
12 x 12 µm² contact





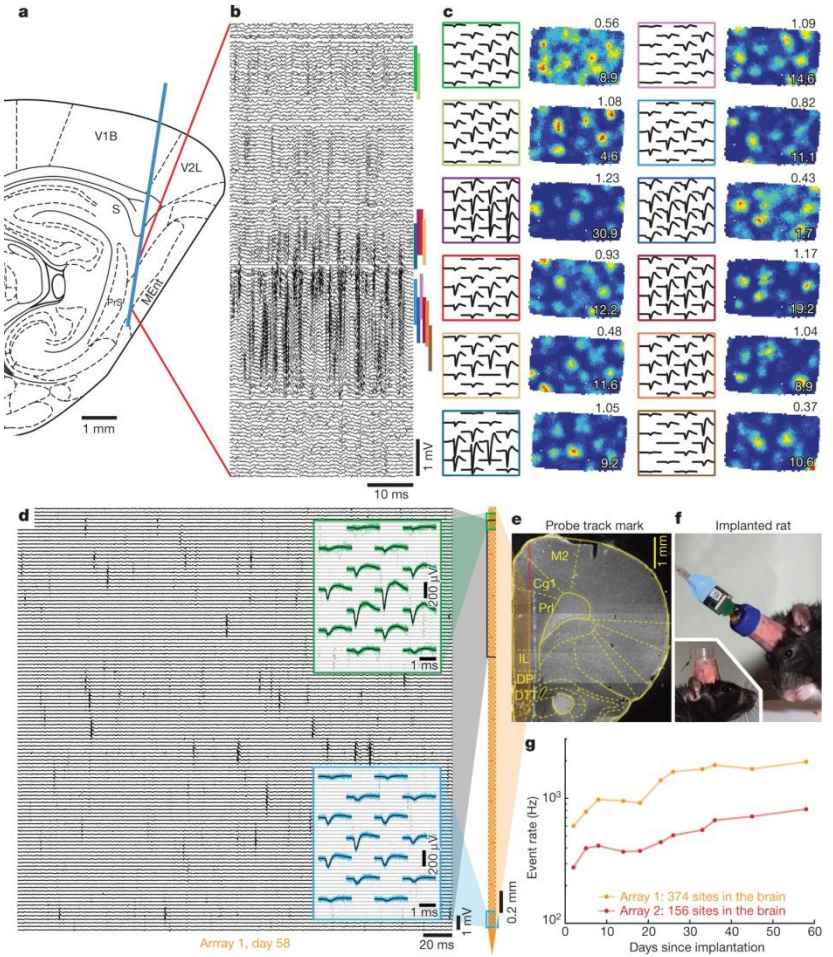
384 sites

149 ± 6 kΩ at 1kHZ

J J Jun *et al. Nature* **551**, 232–236 (2017) doi:10.1038/nature246

Active silicon probes
Neuropixel

Recordings from entorhinal and medial prefrontal cortices using chronic implants in unrestrained rats



J J Jun *et al. Nature* **551**, 232–236 (2017) doi:10.1038/nature246

Take-home messages

- Silicon is a material of choice for microfabricated neural probes

- Leveraging MEMS/microelectronic microfabrication to
  - miniaturise probes
  - integrate on-board processing